ECE4250 Lab 3

State Machine

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# Objective

The objective of this lab was to simulate a state machine that followed the supplied table of states and to use VHDL processes for the model.

# Lab Work

Using Figure 2-56 from the textbook as an example, I designed a two input, clock-controlled state machine based on the table provided. On clock tick rising edge, the machine would check inputs and update the state and output bit based on the x and y bits. The rising edge event is detected by an if statement, and the states are checked using a case statement with four cases and nested if statements to check the four possible xy values and update the state. Outside the process, the output is set to 1 if the state is 2 or 3 and 0 if it is 1 or 0. I ran a simulation using the commands provided, and it produced the expected output.

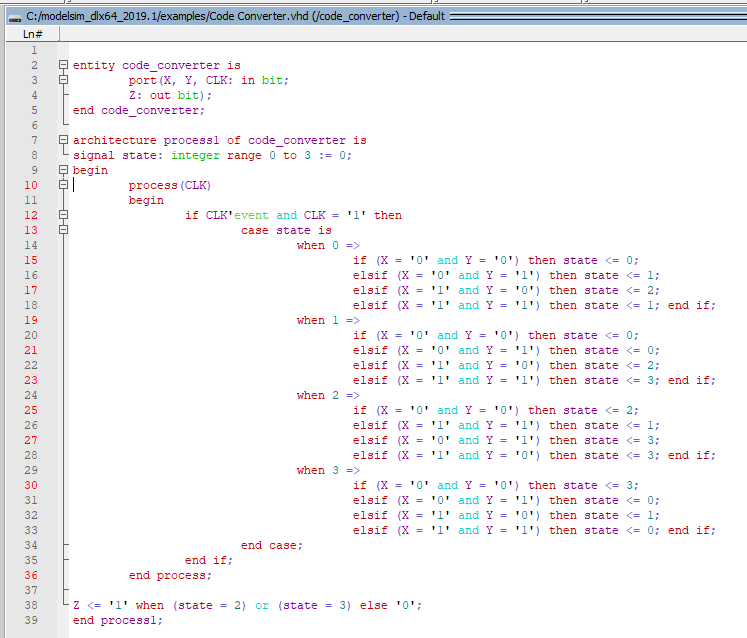


Figure . State machine code

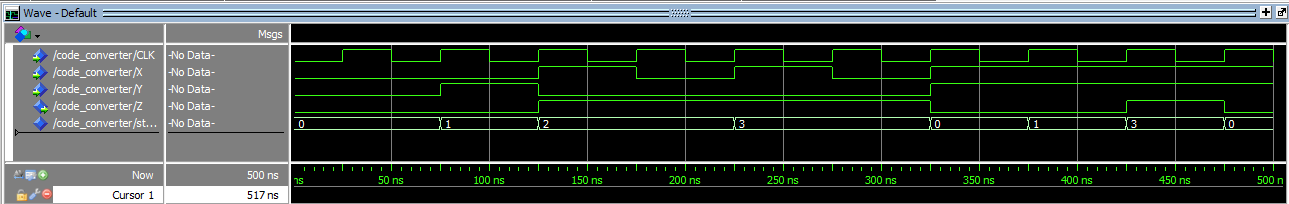


Figure Simulation results

# Conclusion

Using the example in the book made this simulation very straightforward. The only Issue I noticed is that my output graph does not exactly match the one in the lab description. My simulation updates Z immediately but the one in the document appears to update on the next clock cycle. The description in the book for figure 2-56 is that it updates immediately since the Z update is outside the process. Figure 2-54 shows the same machine, but Z in updated in a separate process on clock tick rising edge. It appears that the output I got is correct since the example I was working from did not have Z in a process, and it updates at t+Δ time instead of the next rising edge.

Reference:

C. H. Roth, L. K. John. “Introduction to VHDL,” in *Digital System Design Using VHDL*. 3rd Ed. Boston MA, United States: Cengage, 2016, ch. 2.